WHAT IS CLAIMED IS:

1. A clamp circuit comprising:

a converter that converts an input analog video signal to a digital video signal;

a separation unit that separates a chroma signal and a luminance signal from the digital video signal;

a clamp control circuit that monitors the digital video signal and outputs a clamp control signal in response to a monitoring result of the digital video signal after a predetermined time for extracting a pedestal level inserted in a back porch included in a horizontal banking interval of the analog video signal has elapsed; and

a clamp processing circuit that,

while the clamp control circuit does not output the clamp control signal, extracts the pedestal level from a corrected luminance signal output from the clamp processing circuit, conducts computation processing to converge the extracted pedestal level to a digital signal processing reference level, and corrects the luminance signal input to said clamp processing circuit based on a result of the computation processing to output the corrected luminance signal, and

once the clamp control circuit outputs the clamp control signal, holds a result of the computation processing at the time the clamp control circuit outputs the clamp control signal, and corrects the luminance signal input to said clamp processing circuit based on the held result to output the corrected luminance signal.

2. The clamp circuit according to claim 1, wherein the clamp control circuit comprises:

a signal detection circuit that monitors a change in the digital video signal and outputs a signal detection signal, upon detecting that the digital video signal has changed; and

a delay circuit that delays the signal detection signal by the predetermined time and outputs the delayed signal detection signal as the clamp control signal.

3. The clamp circuit according to claim 1, wherein the clamp control circuit comprises:

a synchronization detection circuit that outputs a synchronization detection signal, upon detecting a horizontal synchronizing signal from the digital video signal; and

a delay circuit that delays the synchronization detection signal by the predetermined time and outputs the delayed synchronization detection signal as the clamp control signal.

4. The clamp circuit according to claim 1, wherein the clamp control circuit comprises:

a synchronization detection circuit that outputs a synchronization detection signal, upon detecting a vertical synchronizing signal from the digital video signal; and

a delay circuit that delays the synchronization detection signal by the predetermined time and outputs the delayed synchronization

detection signal as the clamp control signal.

5. The clamp circuit according to claim 1, wherein the clamp control circuit comprises:

a synchronization detection circuit that outputs a synchronization detection signal, upon detecting a horizontal synchronizing signal from the input analog video signal; and

a delay circuit that delays the synchronization detection signal by the predetermined time and outputs the delayed synchronization detection signal as the clamp control signal.

6. The clamp circuit according to claim 1, wherein the clamp control circuit comprises:

a synchronization detection circuit that outputs a synchronization detection signal, upon detecting a vertical synchronizing signal from the input analog video signal; and

a delay circuit that delays the synchronization detection signal by the predetermined time and outputs the delayed synchronization detection signal as the clamp control signal.

7. The clamp circuit according to claim 1, wherein the clamp processing circuit comprises:

a sampling circuit that extracts sampling data of a pedestal level from a corrected luminance signal based on a clamp pulse input to said sampling circuit at timing of the back porch;

a data averaging circuit that calculates an average of the sampling data of the pedestal level;

a calculating circuit that calculates a difference between the digital signal processing reference level and the average;

a data holding circuit that holds and provides the difference when the clamp control circuit outputs the clamp control signal and provides the difference when the clamp control circuit does not output the clamp control signal; and

a level correction circuit that corrects a level of the luminance signal input to said clamp processing circuit based on the difference provided by the data holding circuit to output the corrected luminance signal.